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JULY 10, 2000

ElectronicNews

SEMICON WEST

Managing ESD in Leading-Edge Fabs

Not having electrostatics management solutions can have shocking results

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ION SYSTEMS

As the cost of semiconductor fabs skyrockets beyond $1.5 billion, fabs must become increasingly automated so that the cost of the factory can be quickly recovered through more efficient manufacturing.

That means that there will be substantially more computing power and huge amounts of data transfers occurring both tool-to-tool and tool-to-host inside fabs.

The operation of the fab will be dependent upon pieces of equipment that can operate as both data appliances and as wafer processors. With thousands of microprocessors now present in a fab, there is a greater range of operating frequencies that are susceptible to an invisible problem: electrostatic discharge (ESD).

In an environment increasingly controlled by centralized computer systems, ESD events can result in electromagnetic interference, causing incomplete data transfers that affect operations throughout the factory, escalating tool downtime and impacting productivity. This, in combination with other technology trends such as smaller feature sizes, 300mm wafers, and the increase in importance and cost of reticles, makes electrostatics management an enabling technology for the manufacture of ICs. The impact of various technology trends on electrostatics is described below.

ESD in the Fab Environment

The fab continues to be an ideal place for static charge to develop and linger. Fabs are full of insulative surfaces that are triboelectrically charged when moved including the wafers and reticles themselves.

An ESD event causes the efficient radiation of an RF burst into the environment and propagates through air or conductors. Almost all ions that make the air conductive and allow static charges on insulative surfaces to dissipate are stripped away by the cleanroom filtration. Depending on the timing of the burst of voltage through nearby equipment or data flows, tools can lock-up, data flows can be corrupted and wafers can be broken.

Tools are packed with microprocessors so that the factory can be fully networked to enable information sharing. These new "data appliances" must exist in a space that is electrostatically and electromagnetically quiet so that information transfers between tools are not interrupted by ESD events or ESD-induced electromagnetic interference (EMI). Electrostatics management solutions enable the electrostatically quiet environment requisite for the fully integrated factory to achieve higher productivity.

Deep Submicron Issues

As the critical dimensions of semiconductor devices reach sub-100-nanometer geometries and some deposited layer thicknesses are driven to atomic scales, it is imperative that electrostatic energy be actively managed in fabs and equipment. Static discharge on surfaces attracts particles at a much higher rate. Wafers with a static charge attract many more particles than wafers with no charge.

In a recent published study, a wafer controlled at 2,000 volts—a charge commonly found in a fab—attracted five times as many particles as a neutral wafer in a class 1 mini-environment over a six-week period. To maximize factory yields and to reduce ESD damage to reticles and wafers, static charge must be controlled.

In the photolithography arena, reticles continue to increase in cost due to increasing complexity (e.g., OPC, phase-shift, etc.). Reticles are also becoming more susceptible to both single catastrophic electrostatic field exposure and lower electrostatic field exposures on a continuous basis, which if not caught, can result in repeating defects on wafers. Unless there is an electrostatics management and control program in place, reticle and product losses will be in the millions of dollars annually. Ionization and other electrostatics control and management methods in the photolithography area can prevent reticles from ESD damage and reduce the frequency of cleaning and repelling. The cost of an electrostatics management program is a fraction of the cost of the problem itself.

The impending move to 157nm photolithography will result in reticles being stored in pure nitrogen environments, aggravating the ESD damage issue already plaguing reticles.

Larger Wafers; Larger Problems

The industry's move to 300mm wafers also presents increased ESD issues. With their larger surface size, 300mm wafers have increased capacitance, which means they can carry significantly more charge than 200mm wafers. Furthermore, the larger size causes an increase in the triboelectric charging between wafers and other objects such as cassettes and robotics. The increased charge due to capacitance and wafer size creates a greater electric field around the wafer that results in greater particle deposition per unit area than on a smaller wafer. When a 300mm wafer loses its charge through an ESD event, the increased amount of discharge in the same timeframe of nanoseconds results in more energy and therefore a much larger EMI event. This more powerful EMI event will reach further and affect the microprocessors in the equipment in the factory.

As fabs become increasingly automated and circuitry design becomes more complex, the need for electrostatics management solutions continues to grow in importance.

ESD and EMI facility evaluations are necessary to allow customers to pinpoint problem areas of the fab and to implement a complete electrostatics management program. Implementation of industry standards and a complete electrostatics management program will increase overall equipment effectiveness and overall factory effectiveness, resulting in higher productivity and increased yield. ESD awareness and management will be a key enabler for the semiconductor industry as it continues toward the push to atomic scales. ■

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Reprinted from **ELECTRONIC NEWS** July 10, 2000